REMARKS

At the time of the Office Action dated June 24, 2004, claims 1-13 were pending. Applicants acknowledge, with appreciation, the Examiner's indication that claims 4-11 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In this Amendment, new claims 14-16 have been added. Care has been exercised to avoid the introduction of new matter. Adequate descriptive support for the new claims can be found in, for example, page 9, lines 19-28 and page 11, lines 15-20 of the specification.

Claims 1-3, 12 and 13 have been rejected under 35 U.S.C. §102(b) as being anticipated by Tomishima et al.

In the statement of the rejection, the Examiner asserted that Tomishima et al. discloses a semiconductor memory device having a power line arranged in a meshed shape identically corresponding to what is claimed. This rejection is respectfully traversed.

The factual determination of lack of novelty under 35 U.S.C. §102 requires the identical disclosure in a single reference of each element of the claimed invention, such that the identically claimed invention is placed into the possession of one having ordinary skill in the art. *Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994). Based on this legal tenet, Applicants submit that Tomishima et al. does not disclose a semiconductor memory device including all the limitations recited in independent claims 1, 12 and 13.

First, Applicants emphasize that the reference does not disclose a semiconductor memory device including "said plurality of memory cell being divided into a plurality of storage units each

formed of the two memory cells bearing complementary data," as recited in the claims (emphasis added).

In the statement of the rejection, the Examiner identified a pair of memory cells MC1 and MC2 in Fig. 3 of Tomishima et al. as the claimed "storage units each formed of two memory cells" (twin-cell). However, in consideration of the arrangement of memory cells shown in Fig. 2 and the bit line voltage waveform during reading shown in Fig. 6, it can be considered that memory cells MC1 and MC2 are for storing independent one-bit data and not forming the twin-cell configuration for bearing complementary data, as claimed. This is so because if memory cells MC1 and MC2 form a storage unit (twin cells) bearing complementary data, voltages of both of complementary bit lines BL and /BL must start varying with a selection of word line WL in the bit line voltage waveform during reading (see Fig. 6 of Tomishima et al.). The bit line waveform obviously shows that each of memory cells MC1 and MC2 stores independent one bit data.

Accordingly, Tomishima et al. does not disclose a semiconductor memory device including "said plurality of memory cell being divided into a plurality of storage units each formed of the two memory cells bearing complementary data," as recited in claims 1, 12 and 13 (emphasis added).

Second, Applicants submit that Tomishima et al. does not disclose a semiconductor memory device including a plurality of cell plates provided corresponding to said storage units, respectively (claims 1 and 13) or corresponding to predetermined sections of said plurality of storage units, respectively (claim 12), and each isolated at least electrically from the others, as recited in the claims. With this limitation, refresh characteristics and manufacturing yields are improved.

In the statement of the rejection, the Examiner asserted that Fig. 3 of Tomishima et al. discloses a plurality of cell plates as claimed. However, it is apparent that Fig. 3 and relevant description of the reference (column 3, lines 50-63) does not disclose, among other things, that a

cell plate is isolated at least electrically from others. In fact, the Examiner did not point out where in Tomishima et al. discloses the above limitation.

Fig. 9 of Tomishima et al. shows a cell plate CPL. However, this cell plate CPL does not correspond to the claimed cell plate. Tomishima et al. in column 13, lines 4-5 mentions, "the cell plate CPL is supplied with a fixed potential (an intermediate potential of Vcc/2, for example)" (emphasis added). Applicants understand that this description teaches that each cell plate is not isolated electrically from others because the cell plate CPL is supplied with the fixed potential. In contrast, because each cell plate is electrically isolated in the claimed invention, each cell plate is not supplied with a specific voltage, and is electrically floated (see page 9, lines 27-28 of the specification).

Accordingly, Tomishima et al. does not disclose a semiconductor memory device including "a plurality of cell plates provided... each isolated at least electrically from the others," as recited in claims 1, 12 and 13 (emphasis added).

The above-described fundamental differences between the claimed invention and Tomishima et al. undermine the factual determination that Tomishima et al. identically describes the claimed invention within the meaning 35 U.S.C. §102. *Minnesota Mining & Manufacturing Co. v. Johnson & Johnson Orthopaedics Inc.*, 976 F.2d 1559, 24 USPQ2d 1321 (Fed. Cir. 1992); *Kloster Speedsteel AB v. Crucible Inc.*, 793 F.2d 1565, 230 USPQ 81 (Fed. Cir. 1986). Applicants, therefore, submit that the imposed rejection of claims 1, 12 and 13 under 35 U.S.C. §102(b) for lack of novelty as evidenced by Tomishima et al. is not factually viable.

It is further submitted that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claim. Therefore, claims 2 and 3 are patentable because they

respectively include all the limitations of independent claim 1. The Examiner's additional comments with respect to claims 2 and 3 do not cure the argued fundamental deficiencies of Tomishima et al.

Based on the foregoing, Applicants respectfully solicit withdrawal of the rejection of claims 1-3, 12 and 13 under 35 U.S.C. §102(b) and favorable consideration thereof.

Conclusion.

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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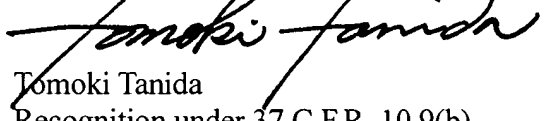

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Recognition under 37 C.F.R. 10.9(b)

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